Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

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1 (currently amended). A digital system comprising a microprocessor, wherein the microprocessor comprises:

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an execution unit;

memory interface circuitry operable to fetch an operand from memory and to provide the operand to the execution unit;

address pointer circuitry operable to provide an address of the operand to the memory interface circuitry; and

modification tracking circuitry connected to the address pointer circuitry, the modification tracking circuitry operable to inhibit a redundant fetch of the operand.

2 (currently amended). The digital system of Claim 1, further comprising a shadow register to hold the operand prior to use by the execution unit.

3 (currently amended). The digital system of Claim 1, wherein the address pointer circuitry is a stand alone coefficient data pointer.

4 (currently amended). The digital system of Claim 1, wherein the execution unit is a multiply-accumulate (MAC) unit.

5 (currently amended). The digital system of Claim 1, wherein a touch instruction "mar(*CDP)" is provided to flag that the operand has been updated in the memory circuit so that the updated operand can be fetched for use by the execution circuit.

6 (currently amended). The digital system of Claim 1, wherein an override mechanism is provided to disable the modification tracking circuitry.

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7 (currently amended). The digital system of Claim 1, wherein ~~coefficient data pointer~~ the modification tracking circuitry is operable to only track address pointer modification during looping operations of the microprocessor.

8 (original). The digital system according to Claim 1 being a cellular telephone, further comprising:

an integrated keyboard connected to the processor via a keyboard adapter;

a display, connected to the processor via a display adapter;

radio frequency (RF) circuitry connected to the processor; and

an aerial connected to the RF circuitry.

9 (original). A method of operating a digital system comprising a microprocessor, comprising the steps of:

loading a data pointer with a first address value;

executing a first instruction in the microprocessor that requires at least a first operand from memory in accordance with the data pointer by fetching the first operand from memory in accordance with the first address value; and

executing a second instruction in the microprocessor that requires at least a second operand from memory in accordance with the data pointer by inhibiting fetching of the second operand from memory if the data pointer has not been modified since the step of executing the first instruction.

10 (original). The method of Claim 9, wherein the step of executing the first instruction comprises loading the first operand into a non-accessible shadow register, such that during the step of executing the second instruction the shadow register is not reloaded if the data pointer has not been modified since the step of executing the first instruction.

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11 (original). The method of Claim 9, further comprising the step of loading the data pointer with a second address value between the step of executing the first instruction and the step of executing the second instruction; and

wherein the step of executing the second instruction comprises fetching the second operand from memory in accordance with the second address value.

12 (new). The digital system of Claim 1, wherein the address pointer circuitry comprises:

a pointer register for storing at least a portion of a memory address of the operand;

wherein the memory interface circuitry fetches operands from memory using the contents of the pointer register for at least a portion of the memory address.

13 (new). The digital system of Claim 12, wherein the modification tracking circuitry is for detecting modifications to the memory address of an operand occurring during the execution of instructions by the execution unit, and inhibits a fetch of an operand responsive to the execution unit executing an instruction that uses the fetched operand and that does not modify the memory address of the operand stored in the pointer register.

14 (new). The digital system of Claim 12, wherein the execution unit comprises a multiply-accumulate (MAC) unit.

15 (new). The digital system of Claim 12, wherein the execution unit comprises a plurality of multiply-accumulate (MAC) units.

16 (new). The digital system of Claim 1, wherein the execution unit comprises a plurality of multiply-accumulate (MAC) units.